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(54) Improvements in telephone instruments

(57) In a control circuit for the two speech paths of a hands-free telephone, logarithmic analog to digital converters 133,134 generate digital words corresponding to the signal amplitudes on the two paths. These words are compared with stored references in decision logic and the relative attenuation of the paths is adjusted by switched attenuators 131,132 according to the result of this comparison. The total loop gain is maintained substantially constant.

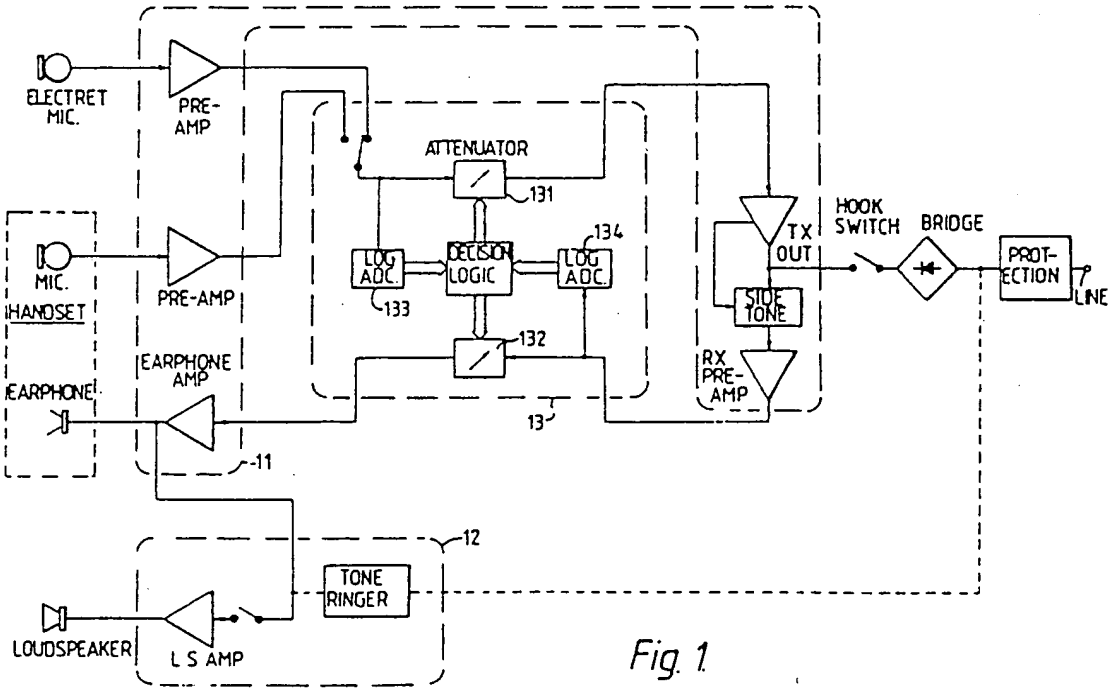

Fig. 1

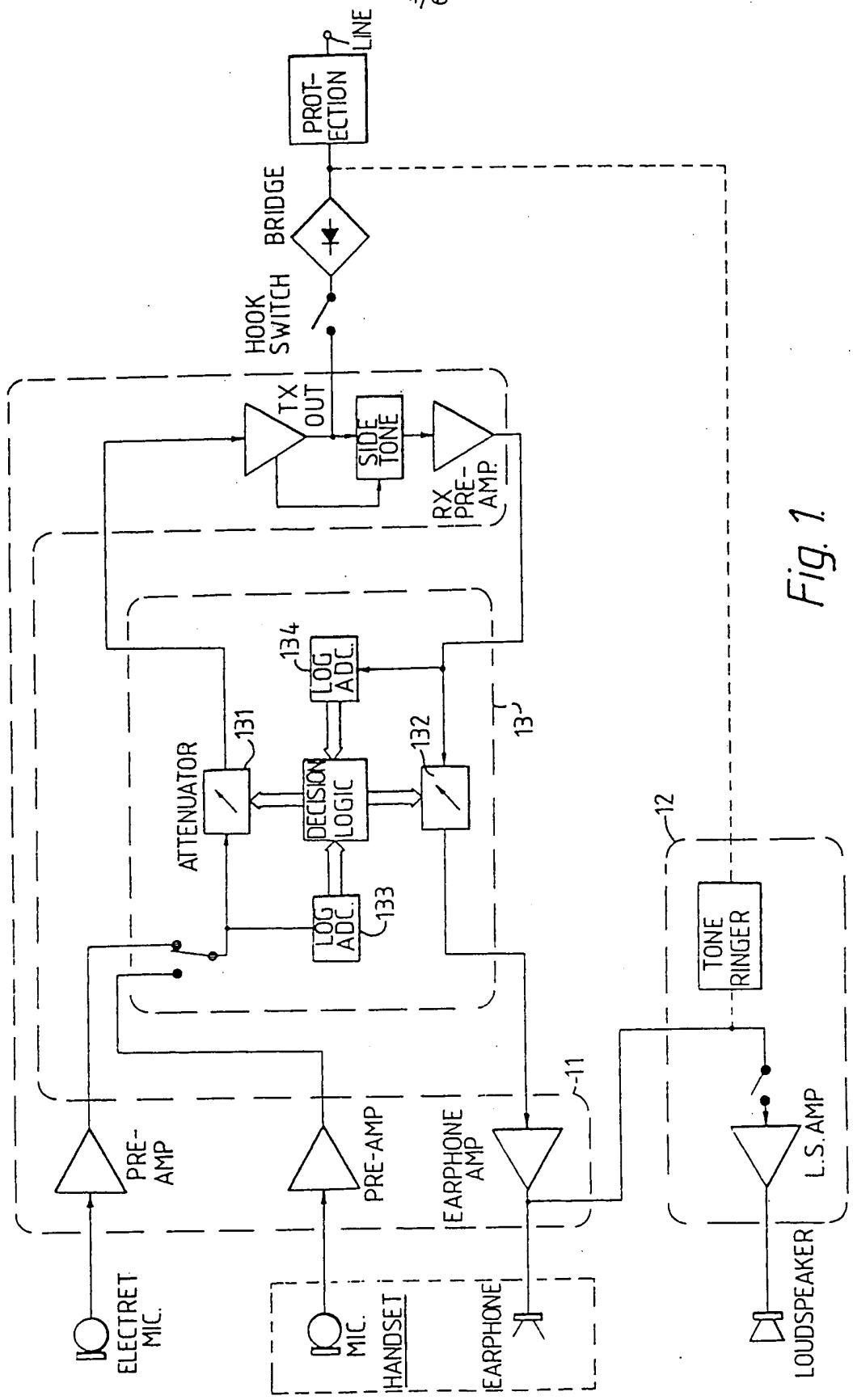
LINE
PROT-ECTION
BRIDGE
HOOK SWITCH
TX OUT
SIDE TONE
RX PRE-AMP
134
LOG ADC.
131
ATTENUATOR
DECISION LOGIC
132
13
LOG ADC.
133
12
TONE RINGER
PRE-AMP
PRE-AMP
EARPHONE AMP
11
L.S.AMP
ELECTRET MIC.
MIC.
HANDSET
EARPHONE
LOUDSPEAKER

Fig. 1

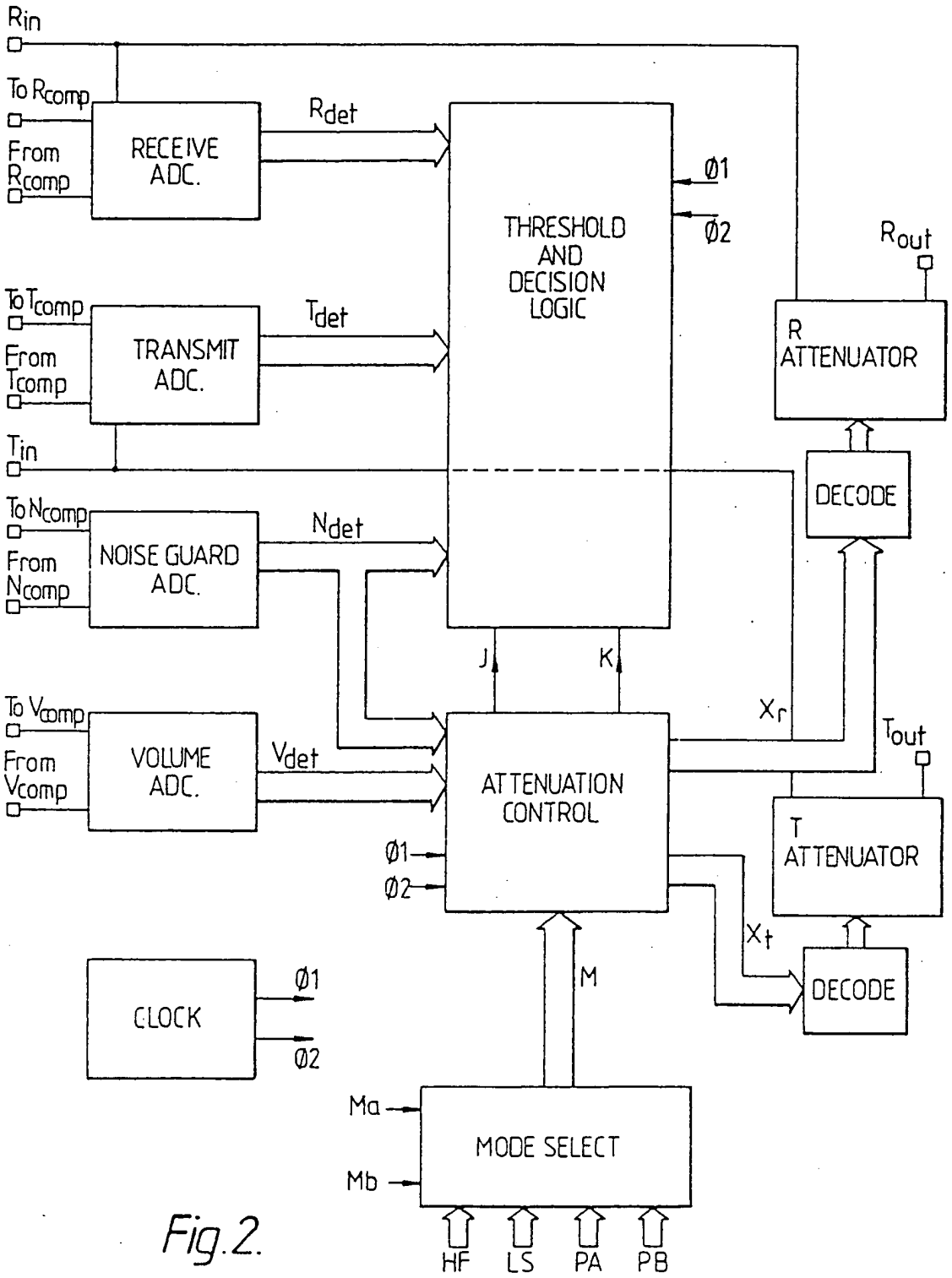
Rin
To Rcomp
From Rcomp
RECEIVE ADC.
Rdet
THRESHOLD AND DECISION LOGIC
Ø1
Ø2
Rout
R ATTENUATOR
To Tcomp
From Tcomp
TRANSMIT ADC.
Tdet
Tin
DECODE
To Ncomp
From Ncomp
NOISE GUARD ADC.
Ndet
J
K
To Vcomp
From Vcomp
VOLUME ADC.
Vdet
ATTENUATION CONTROL
Xr
Tout
T ATTENUATOR
Ø1
Ø2
Xt
DECODE
M
CLOCK
Ø1
Ø2
Ma
Mb
MODE SELECT
HF
LS
PA
PB

Fig.2.

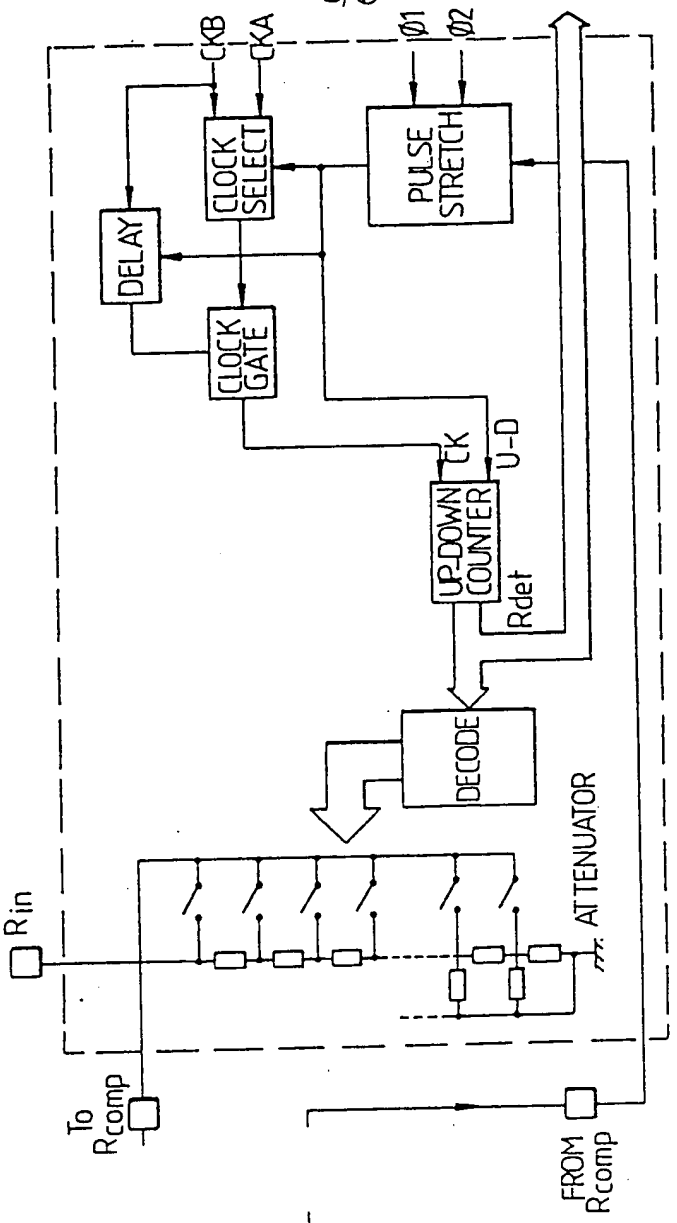
CKB
CKA
Ø1
Ø2
CLOCK SELECT
PULSE STRETCH
DELAY
CLOCK GATE
CK
U-D
UP-DOWN COUNTER
Rdet
DECODE
ATTENUATOR
Rin
To Rcomp
FROM Rcomp

Fig.3.

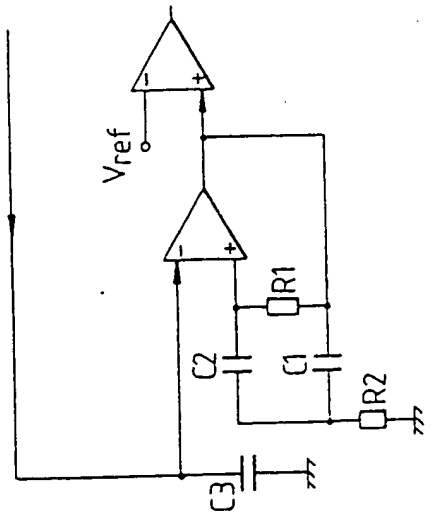
Vref
R1
C2
C1
R2
C3

Fig.4a.

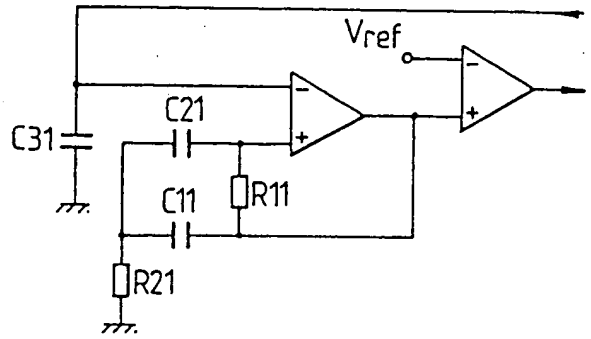

Fig. 4b.

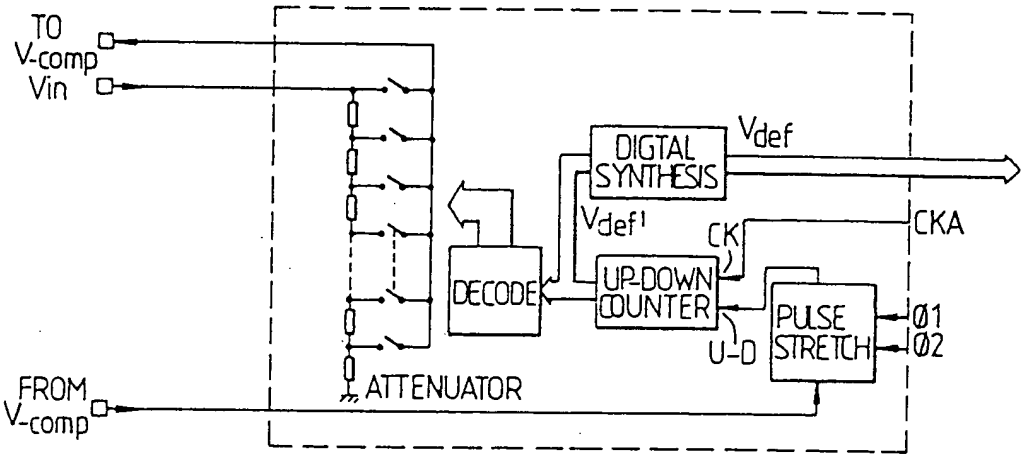

Fig. 5a.

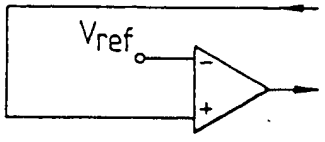

Fig. 5b.

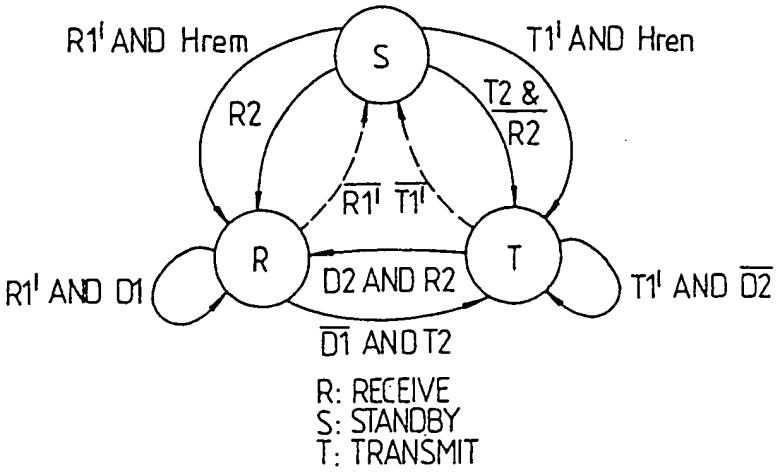

Fig. 6. STATE DIAGRAM FOR DECISION LOGIC

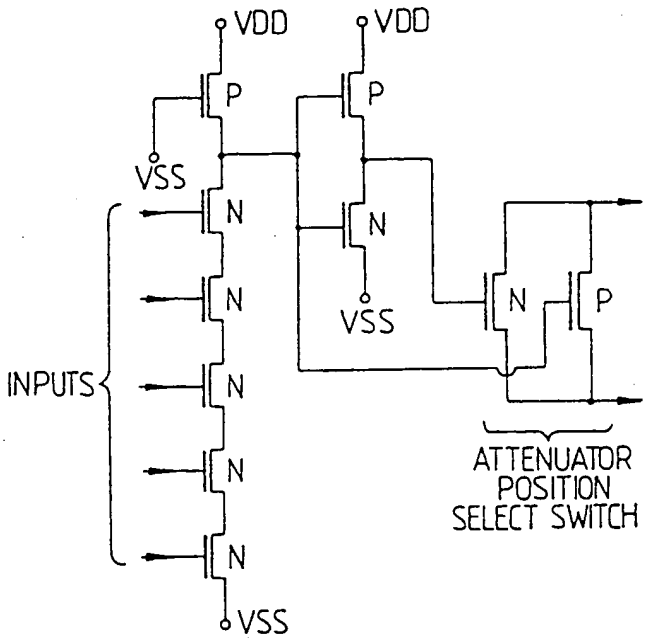

Fig. 8.

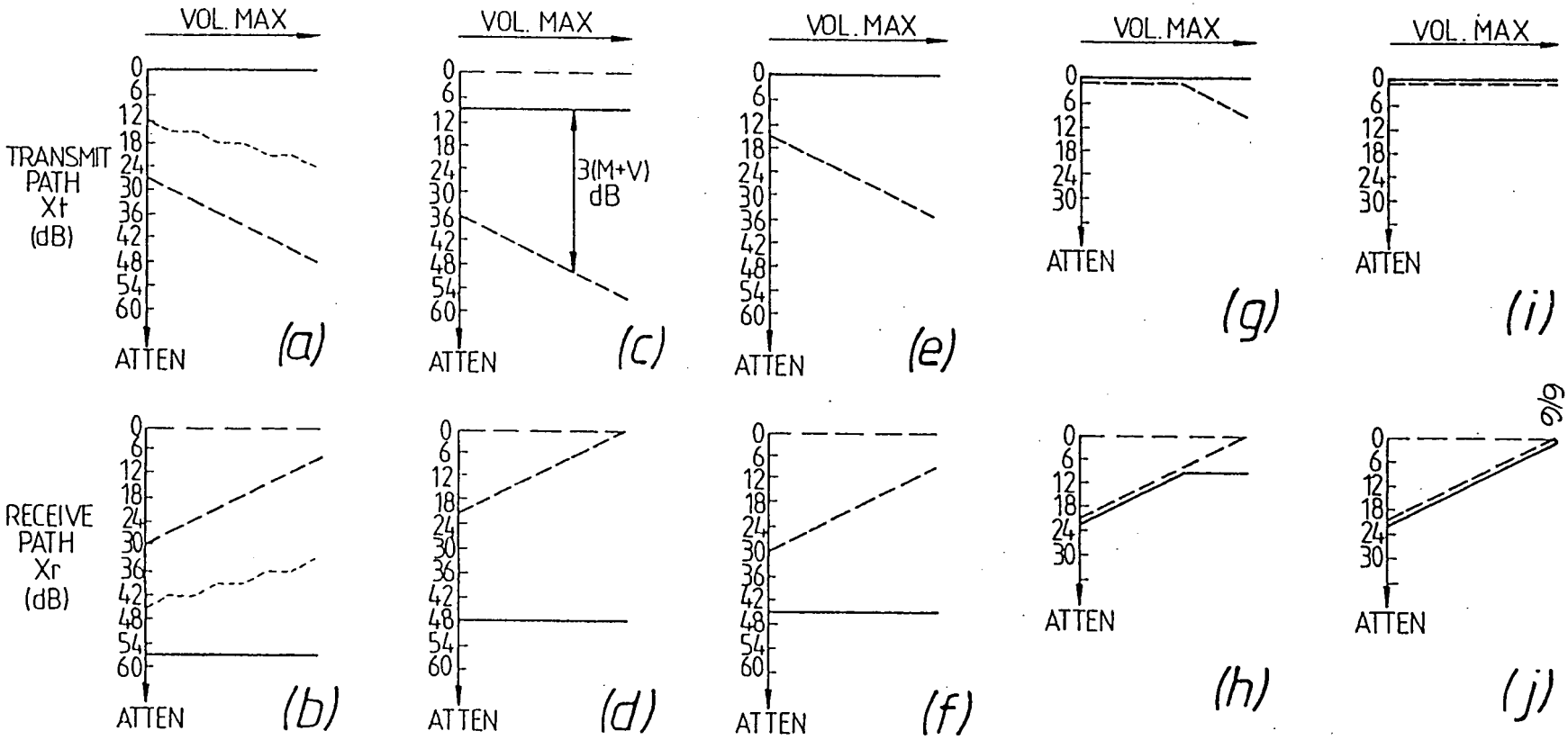

Fig.7.

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SPECIFICATION

Improvements in telephone instruments

This invention relates to telephone instruments and in particular to the provision of hands-free and loudspeaking operation in such instruments. A telephone subset in its simplest form consists of a transmit path, a receiver path and a circuit to interface the two-wire subscriber line to the four-wire subset, referred to as a 2 to 4 wire converter, line-interface circuit, or simply as a network. In general the subset transmit path is a microphone and amplifier, and the receive path is an amplifier driving an earpiece or loudspeaker. In a hands-free instrument the loudspeaker and microphone may be in the same case.

For handsfree operation the instrument specification requires certain gains for the transmit and receive paths, and also imposes a maximum return loss, i.e. the fraction of the signal coming in one the line which reappears as a transmit signal to the line. Due to acoustic coupling from loudspeaker to microphone an attenuated version of the receive signal appears in the transmit path. Acoustic coupling occurs through the housing if loudspeaker and microphone are in the same case, and via reflections from the room. Therefore to meet required gain levels and return loss some attenuation must be inserted in the loop. The attenuation is shifted from one path to the other in response to speech levels. Because the line interface network is not ideal, there is also some sidetone coupling which causes the transmit signal to appear in the receive path. Thus the switched attenuation is also required to keep the total gain round the subset itself below unity, so that instability cannot occur. In practice, however, it is usually return loss that determines how much attenuation has to be inserted.

In the past handsfree instruments have been built with discrete analog circuitry, using simple switches as attenuators. Such an instrument uses many discrete components and therefore is expensive. Furthermore, because of the simple switching systems and the analog circuitry at present employed the handsfree performance may be far from optimum.

The object of the invention is to minimise or to overcome these disadvantages.

According to the invention there is provided a circuit for the controlled attenuation of the transmit and receive speech paths of a hands-free telephone instrument, the circuit including logarithmic analog to digital converters, one for each speech path, switched attenuators one in each speech path, and a decision logic circuit whereby said attenuators are controlled, wherein each analog to digital converter is adapted to generate a digital word corresponding to the signal amplitude on its respective speech path, wherein said decision logic is adapted to compare the two words and to determine the relative attenuation of the two speech paths in response thereto such that the total loop gain is maintained substantially constant.

An embodiment of the invention will now be described with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram of a telephone instrument incorporating the control circuit;
Figure 2 is a schematic diagram of the control circuit;
Figure 3 shows the construction of the analog to digital converters of the circuit of Fig. 2;
Figures 4a and *4b* show the off-chip circuitry associated with the analog to digital converters of Fig. 3;
Figures 5a and *5b* show a volume control analog to digital converter for use with the circuit of Fig. 2.
Figure 6 is a state diagram for the decision logic of the control circuit;
Figures 7a to *7j* illustrate the operation of the signal path attenuators of the control circuit and
Figure 8 shows the circuitry of a decoder stage.

Referring to Fig. 1, the telephone circuit includes three integrated circuits comprising an operating circuit 11, which provides the basic telephone functions, an audio output circuit 12 for loudspeaking and tone ringing factors, and a control circuit 13 for the controlled attenuation of transmit and receive speech paths in hands-free operation. The operation of the circuit 11 is described in our co-pending application No. 8317706 (P.F. Blomely et al 11-7-3-1) and the operation of the circuit 12 is described in our co-pending application No. (A. Lefevre 2). It will be clear however that use of the control circuit 13 is not limited to the particular circuits 11 and 12 shown in Fig. 1.

The control circuit 13 includes attenuators in the transmit path 121 and receive path 132 which attenuators are digitially controlled in response to detected transmit and receive voice signal levels (Tdet and Rdet). They consist typically of simple resistor chains and are logarithmic with a step size e.g. of 3dB and a maximum attenuation of 69dB.

The attenuators can be in one of three stable states
State R : R path "on" and T path "off"
State T : T path "on" and R path "off"
State S : Both attenuators half-way between the on and off positions.

Four modes of operation are available, for selection by the user:—

HF—Hands-free mode
LS—Loudspeaking mode using handset microphone
PA—Plain ordinary telephone (or handset) mode
PB—Handset mode with a small amount of voice controlled attenuation.

The amount of signal path attenuation switched in each mode in going from state R to state T is called the total depth of switching, and may be preselected by metal mask option. In mode PA the depth of switching will normally be zero. Mode PB is provided for certain subsets where return loss may be marginal even in handset mode.

A user operated receive volume control may be provided by adjusting the "on" attenuation of the R path. It also adjusts the depth of switching so that there is less switching at reduced volume. For any given mode and volume setting the total depth of switching is kept constant at all times, at a value which is known to be sufficient to meet to return loss requirements.

The digital words representing the magnitude of Rdet and Tdet signals (and also noise and volume signals, see below) are determind by A to D converters 133 and 134. The attenuators and logic for the ADC function are on-chip, the ADC comparators are off-chip. The signal ADCs perform the function of half-wave rectification and peak following, and generate a logarithmic digital representation of the signals with a step size (one bit) of 3dB and a dynamic range of 69dB. The dynamics, or timing, of ADC operations (rate of following on signal attack and decay) may be preselected by metal mask option from a sequence of timing waveforms derived by repeated division-by-two from a basic clock. The clock is generated on-chip, with an external R and C to define frequency.

The state (R, T or S) is determined by the magnitude of the digital words representing Rdet and Tdet relative to thresholds. There are six thresholds:

Upper and lower absolute thresholds for Rdet
Upper and lower absolute thresholds for Tdet
Two differential thresholds, which are compared with (Rdet-Tdet).

All six thresholds may be preselected by metal mask options. Two are provided in each case so that there is hysteresis in the decision logic. When both Rdet and Tdet are below their absolute thresholds the state is S (standby), and when both Rdet and Tdet are above their absolute thresholds the state is R or T, depending on the magnitude of (Rdet-Tdet) relative to the differential thresholds.

Following a change of state from S or R or S to R or R to/from T, the signal path attenuators perform a "fast" ramp through their steps. Following a change from state R to S or T to S there is a "hold" time followed by a "slow" ramp through the steps. At all times the R path and T path attenuators move together so that total loop gain is constant. Fast and slow ramp rates and hold time are preselected by metal mask options from the sequence of timing waveforms mentioned above. The hold and slow ramp that follow a change to standby means that the attenuators do not respond to small pauses the occur in normal speech: this is essential to avoid speech 'break up" which would be subjectively very undesirable. At the same time the fast ramp action that occurs for all other transitions prevent loss of leading syllables from speech.

In HF mode there is an automatic noise guard function which responds to steady background noise on the transmit (room) signal. The noise ADC has slow attack and fast decay characteristic. Increasing room noise increases T path "on" attenuation and reduces R path "on" attenaution, and modifies absolute thresholds so that they stay above room noise level.

Fig. 2 is a schematic diagram of the control circuit which consists of eight major blocks:

Logic and attenuator for the transmit signal ADC
Logic and attenuator for the receive signal ADC
Logic and attenuator for the noise guard ADC
Logic and attenuator for the volume control ADC
Threshold and decision logic
Attenuator control logic
Clock generator
Mode select

In addition there are the two signal path attenuators. Typically the circuit is fabricated in ISOCMOS technology, using a standard cell library for most of the logic, and custom layout for the attenuators and their decoders.

The A to D Converter Circuits

These are shown in Fig. 3.

R and T Signal ADCs

Only the logic and attenuator for the ADC are on the chip, with the comparator and reference voltage off-chip. Fig. 4a shows the R path ADC with its off-chip circuitry. The heart of the logic is a five bit up-down counter whose output Rdet is a five bit word corresponding to the digital conversion of the signal level. Rdet is decoded to control the attenuator, so that Rdet = 0 gives zero attenuation and Rdet = 23 gives maximum attenuation. A speech signal is applied at R_{in} and in attenuated version of it appears at the "To R-comp" pin. The signal is amplified, filtered

and compared with a reference voltage Vref. If the negative-going peaks of the signal are less than Vref at this point then the comparator sends a steady logic 1 to the "From R-comp" pin. The ADC logic responds by incrementing the counter, i.e. Rdet, one count downwards, so the signal at "T R-comp" is now larger. This process continues until a negative-going peak at the comparator exceeds Vref. The comparator output now goes to logic 0 at each signal peak, and the logic responds by incrementing Rdet one count up. Therefore if a steady tone is applied at R_{in}, the "steady state" response of the ADC is to have Rdet hopping continually between two adjacent values. This is not a problem because hysteresis is incorporated in other parts of the logic.

The logic includes delay and clock select circuits. When an up count is required CKA is selected to drive the counter; this is a relatively fast clock. When a down count is required CKB, which is much slower, is selected, and also a delay is initiated before any CKB pulses are enabled. This gives the ADC its fast attack and slow decay characteristics, so that it is in effect a peak follower. The pulse stretcher circuit in the logic input is used to "clean up" the waveform from the comparator, so that very short or noisy bursts of pulses cannot cause logic malfunction. External amplifier gain and Vref are chosen so that the ADC's dynamic range could embrace signals from about 1.7mV peak to 3V peak. In practice signals above approximately 1 volt peak do occur, so the whole ADC dynnamic range is not used.

Noise Guard ADC

The noise guard ADC operates on the same principle as the signal ADC's but it has only an 8 position attenuator, Ndet having values in the range 0 to 7. The off-chip circuitry is slightly different, as shown in Fig. 4b. In this case when the count direction is up a very slow clock, CKC, is steered to the counter, and when the count is down CKD, which is somewhat faster, is selected; in both cases there is a delay before clock is enabled. Thus the noise ADC has a very slow attack and relatively fast decay, so that it tends to sit at the peak level of any steady continuous signal at Ncap, and is unable to respond to speech signals. The signal at Ncap is a low-pass filtered version of T_{in}. Thus Ndet represents any continuous low frequency background noise in the room. As before, with a steady input Ndet hops between two adjacent values. In this case digital hysteresis has to be included so that the 3 bit word Ndet routed to the rest of the logic is constant with steady room noise. Ndet has values in the range 1 to 7, giving noise guard action effectively over a range typically of 18dB. The amount of extra attenuation added to Tpath or removed from Rpath by the noise guard is Ndet/2, and so is at most 9dB.

Volume control ADC

Receive volume has to be controlled by a d.c. voltage derived from a potentiometer; hence an ADC is also required for volume. As can be seen from Figs. 5*a* and 5*b*, this is a simplified version of the other ADCs. The attenuator has resistor values in a hyperbolic (reciprocal) progression, so that steps are evenly spaced if a linear volume potentiometer is used. There is only one clock and no delay. Digital hysteresis is again used to eliminate "hopping". If the d.c. level at Vin is such that the ADC is on the borderline between two steps the system is liable to move randomly between these steps, in addition to the "hopping" which occurs as described above. A hysteresis of two steps is used to eliminate this. The 3 bit word Vdet taken to the rest of the logic has a range of 8 values, from 0 to 7, with 7 corresponding to maximum volume, giving a volume control range typically of 21db.

Threshold and Decision Logic

The threshold and decision block takes the 5 bit words Rdet and Tdet, compares them with preset threshold values, and decides what state the subset should be in. Its functions can be summarised as follows:—

Rth, Tth and Hyst are preset words which set the absolute threshold.

Lower R absolute threshold : Rth1 = Rth = Ndet/2
Upper R absolute threshold : Rth2 = Rth1 + Hyst
Lower T absolute threshold : Tth1 = Tth + Ndet
Upper T absolute threshold : Tth2 = Tth1 + Hyst

If Rdet > or = Rth1 then R1 = 1, else R1 = 0.

Similarly for R2, T1 and T2. R1 and T1 are re-timed versions of R1 and T1, to avoid the problem of speech break-up.

Dth1 and Dth2 are preset words for the differential thresholds. The 5 bit word Ix and logic signals J and K come from the attenuator control block. J and K are set by the depth of switching and are used to adjust Dth1 and Dth2.

The decision logic takes inputs R1, R2, T1, T2, D1, D2 and Hrem, to make the decision as to whether state should be R, S or T. The state diagram in Fig. 6 defines the decision logic in

detail. Hrem is the logic signal from attenuator control which briefly removes absolute hysteresis. A three-level output is provided from a single pad to indicate state. This is advantageous for circuit test and evaluation.

Mode Select

The two logic inputs Ma and Mb determine the mode of operation by selecting one of the 5 bit words HF, LS, PA or PB which are preset on the chip, as shown in the Table below. The value of "Mode" thus selected determines the depth of switching. This block also provides Ma which together with Mb selects input Tin1 or Tin2. If the mode is Hands-free, the transmit path is connected to the pre-amp for the electret microphone in the subset body. For the other modes the handset microphone pre-amp is selected.

Ma	Mb	Typical value of Mode (M)	Operation
0	1	9	HF: HANDSFREE
1	1	5	LS: LOUDSPEAKING
0	0	25 (=-7)	PA: HANDSET
1	0	28 (=-4)	PB: HANDSET WITH SWITCHING

Attenuator Control

The attenuator control block sets up two 5 bit words Xt and Xr which drive the signal path attenuators. They can have values from 0 to typically 23, where 0 gives zero attenuation and 23 gives e.g. 69dB of attenuation. Inputs to this block are Ndet, Vdet, Mode and the three state lines R, S and T from the decision logic. For a given operating mode and receive volume setting the depth of switching is constant.

The signal path attenuators are controlled as follows: Xt is compared at all times with a 5 bit word Ix, the value of which is set by the state. When Xt = Ix the signal path attenuators are in the correct position and the value of Xt is held there. When Ix takes a new value, Xt follows it under control of the appropriate clock, until Xt = Ix again.

If mode is HF or LS:—

In transmit state, T : Xton = Ix = I1 = Ndet/2

In receive state, R : Xtoff = Ix = I3 = Ndet/2 + M + V

In standby state, S : Xtsty = Ix = I2 = (I1 + I3)/2

If mode is PA or PB:—

Xton = I1 = 0

Xtoff = I3 = M + V

Xtsty = I2 = (I1 + I3)/2

Obviously, when mode is PA or PB and V = 0 then I1 = I2 = I3 = 0 and Xt = 0 at all times.

Xr is derived from Xt. When Xt = Xt then $Xr = Xr_{off}$, and vice versa. Xr is calculated by inverting the Xt word and adding it either to M or to the inverse of V, and a constant Q. Q can take one of four values depending on mode and on whether or not M = V is zero. The values of Q are chosen to put Xr in the required position, and depend on the fact that the five bit word Xr "re-cycles" when it exceeds its maximum value.

The operation of the attenuation control is shown in Figs. 7a to 7j which show the "on", "off" and "standby" position of signal path attenuators as a function of receive volume, for the four operating modes. The effect of noise guard is also shown.

The 5 bit word Xt is generated with an up-down counter in a manner very similar to that used in the ADCs. When the new state is R or T a relatively fast clock, CKE, is steered to the counter so that signal path attenuators make a fairly fast transition to their new position. When the new state is S a slower clock, CKF, is selected, giving a slow ramp rate back to standby. Before the slow ramp is initiated there is a delay or about seven CKG periods to give the "hold" time that precedes a return to standby.

Clock Generator

The clock generator controls all timing on the chip. It may consist of a simple relaxation oscillator with off-chip resistor and capacitor to set the frequency, followed by a two phase generator for 01 and 02. These are non-overlapping pulse trains which drives most of the logic.

There follows a number of stages of frequency division with 01 as input, to provide a wide range of clock waveforms from which the clocks to control specific timing requirements on the chip can be selected. Seven different clock waveforms, labelled CKA to CKG, are needed for various parts of the logic; a connection matrix allows them to be selected from any of the 16 stages by metal mask option.

Attenuators and Decoders

Attenuators

The chip contains six attenuators with decoders, two signal path attenuators plus one for each of the four ADCs. All attenuators except volume control have e.g. 3dB step increments. For the noise ADC an 8 step attenuator may be used, and for volume ADC, 10 steps. They are simple series resistor chains. The other four attenuators all have preferably 23 steps, and are more conveniently made with series resistors for the top half of the chain and an R-2R network for the bottom half.

Decoders

Fig. 8 is the circuit of a 5-bit decoder stage. Preferably it is made with "pseudo NMOS" rather than a full complementary circuit, thus saving considerable area. A decoder normally has its drive transistors in parallel so that all are off when a stage is selected, and static current flows in all the rest of the stages. To avoid this large current drain decoders on the present circuit use series drive devices; now "all on" selects the stage, and only the selected stage draws current. The P-channel load device is electrically small, giving current drain of typically 3uA for the whole decoder. The method is feasible because the slow response of such a structure does not matter in this application.

Whilst the circuit described herein is intended for use in a telephone instrument it will be apparent that it is not so limited and can be employed in other applications such as intercom systems.

CLAIMS

1. A circuit for the controlled attenuation of the transmit and receive speech paths of a hands-free telephone instrument, the circuit including logarithmic analog to digital converters, one for each speech path, switched attenuators one in each speech path, and a decision logic circuit whereby said attenuators are controlled, wherein each analog to digital converter is adapted to generate a digital word corresponding to the signal amplitude on its respective speech path, wherein said decision logic is adapted to compare the two words and to determine the relative attenuation of the two speech paths in response thereto such that the total loop gain is maintained substantially constant.

2. A circuit for the controlled attenuation of the transmit and receive speech paths of a hands-free telephone instrument, the circuit including logarithmic analog to digital converters, one for each speech path, a noise guard analog to digital converter, switched attenuators one in each speech path, a decision logic circuit whereby said attenuators are controlled, and a clock for providing timing signals to the analog to digital converters and to the decision logic circuit, wherein the transmit and receive analog to digital converters are adapted to generate digital words corresponding to the relative signal amplitudes on the two speech paths, wherein the decision logic circuit is adapted to compare said words with stored predetermined words and thereby to determine the relative attenuation to be inserted in the two speech paths, wherein the noise guard analog to digital converter is adapted to generate a further digital word in response to a substantially continuous background noise signal on the transmit path whereby the decision logic increases the transmit path attenuation and decreases the receive path attenuation, the arrangement being such that the relative attenuation of the receive and transmit paths provides a substantially constant total loop gain.

3. A circuit as claimed in claim 2, and incorporating a volume control analog to digital converter whereby attenuation is transferred from the receive path to the transmit path.

4. A circuit as claimed in claim 2 or 3, wherein each said analog to digital converter compares an input signal with a reference voltage, attenuates that signal such that the attenuated signal peak values correspond to the reference voltage.

5. A circuit as claimed in claim 4, wherein each said digital word is generated by an up-down converter from a comparison of a clock signal and a digital signal corresponding to the attenuated speech signal.

6. A circuit as claimed in any one of claims 1 to 5, and in the form of an integrated circuit.

7. A circuit for the controlled attenuation of the speech paths of a hands-free telephone, which circuit is substantially as described herein with reference to the accompanying drawings.

8. A telephone instrument provided with a control circuit as claimed in any one of claims 1 to 7.

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